

First Named Inventor	Frankie F. Roohparvar	COMMUNICATION REGARDING CERTIFICATE OF CORRECTION
Patent No.	6,873,564	
Issue Date	March 29, 2005	
Examiner Name	Trong Q. Phan	
Attorney Docket No.	400.006US02	
Title: ZERO LATENCY-ZERO BUS TURNAROUND SYNCHRONOUS FLASH MEMORY		

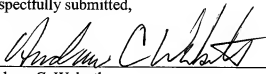
Attention Certificate of Corrections Branch
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P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby requests issuance of a Certificate of Correction in U.S. Letters Patent No. 6,873,564 as specified on the attached four Certificates of Correction Forms (PTO/SB/44).

Applicant believes these corrections are necessary due to Applicant's errors of a clerical nature and authorizes the payment of the \$100.00 Certificate of Correction fee from Deposit Account 501373. If deemed necessary, the U.S. Patent Office is authorized to charge any additional fees found due to our Deposit Account No. 501373. Please contact the undersigned attorney if you have any questions.

Respectfully submitted,

Date: 2/23/07


Andrew C. Walseth
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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 4

PATENT NO. : 6,873,564
APPLICATION NO.: 10/779,425
ISSUE DATE : March 29, 2005
INVENTOR(S) : Roohparvar

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, Line 47, delete "Many modern personal" and insert --Many modern personal--

Column 8, Line 8, delete Table 1:

and insert Table 1:

TABLE 1

BURST DEFINITION				
Order of Accesses Within a Burst				
Burst Length	Starting Column Address	Type = Sequential	Type = Interleaved	
2	A0	0-1	0-1	
	1	1-0	1-0	
4	A1	A0		
	0	0-1-2-3	0-1-2-3	
	0	1-2-3-0	1-0-3-2	
	1	0-2-3-0-1	2-3-0-1	
	1	3-0-1-2	3-2-1-0	
8	A2	A1		
	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	
	0	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	
	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	
	0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	
	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	
	0	5-6-7-0-1-2-3-2	5-4-7-6-1-0-3-2	
	1	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	
	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	
0	1			
0	1			
0	1			
1	0			
1	0			
1	1			
1	1			
1	1			
1	1			
Full	n = A0-A7	Cn, Cn + 1, Cn + 2	Not supported	
Page 256	(location 0-255)	Cn + 3, Cn + 4, ... Cn - 1, Cn ...		

TABLE 1

BURST DEFINITION				
Order of Accesses Within a Burst				
Burst Length	Starting Column Address	Type = Sequential	Type = Interleaved	
2	A0	0-1	0-1	
	0	1-0	1-0	
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	0	0-1-2-3	0-1-2-3	
	0	1-2-3-0	1-0-3-2	
	1	0-2-3-0-1	2-3-0-1	
	1	3-0-1-2	3-2-1-0	
8	A2	A0		
	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	
	0	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	
	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	
	0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	
	1	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	
	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	
	1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	
	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	
	1	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	
	1	5-6-7-0-1-2-3-2	5-4-7-6-1-0-3-2	
	1	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	
	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	
Full	n = A0-A7	Cn, Cn + 1, Cn + 2	Not supported	
Page 256	(location 0-255)	Cn + 3, Cn + 4, ... Cn - 1, Cn ...		

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Leffert Jay & Polglaze, PA
P.O. Box 581009
Minneapolis, MN 55458-1009

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 10 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 2 of 4

PATENT NO. : 6,873,564
APPLICATION NO.: 10/779,425
ISSUE DATE : March 29, 2005
INVENTOR(S) : Roohparvar

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Columns 9 and 10, Line 33, delete Table 2:

TRUTH TABLE 2															
Flash Memory Command Sequences															
Operation	1 st CYCLE					2 nd CYCLE					3 rd CYCLE				
	CMD	ADDR	ADDR	DQ	RP#	CMD	ADDR	ADDR	DQ	RP#	CMD	ADDR	ADDR	DQ	RP#
READ DEVICE	LCR	90H	Bank	X	H	ACTIVE	Row	Bank	X	H	READ	CA	Bank	X	H
Config READ	LCR	70H	X	X	H	ACTIVE	X	X	X	H	READ	X	X	X	H
Status Register CLEAR	LCR	50H	X	X	H										
Status Register ERASE	LCR	20H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	00H	HV _{OUT}
SETUP/ Confirm	LCR	40H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	Col	Bank	DIN	HV _{OUT}
WRITE SETUP/ WRITE	LCR	60H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	01H	HV _{OUT}
Protect BLOCK/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	01H	V _{OUT}
Protect DEVICE/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	02H	HV _{OUT}
Unprotect BLOCKS/ Confirm	LCR	30H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	03H	H
ERASE NVmode Register	LCR	A0H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	X	H
WRITE NVmode Register	R	H	k			VE	k		E	k					

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Columns 9 and 10, Line 33, insert Table 2:

TRUTH TABLE 2															
Flash Memory Command Sequences															
Operation	1st CYCLE					2nd CYCLE					3rd CYCLE				
	CMD	ADDR	ADDR	DQ	RP #	CMD	ADDR	ADDR	DQ	RP #	CMD	ADDR	ADDR	DQ	RP #
READ DEVICE Config.	LCR	90H	Bank	X	H	ACTIVE	Row	Bank	X	H	READ	CA	Bank	X	H
READ Status Register	LCR	70H	X	X	H	ACTIVE	X	X	X	H	READ	X	X	X	H
CLEAR Status Register	LCR	50H	X	X	H										
ERASE SETUP/Confirm	LCR	20H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	DQH	H/V _{SET}
WRITE SETUP/Confirm	LCR	40H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	Col	Bank	DIN	H/V _{SET}
Protect BLOCK/Confirm	LCR	60H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	OH	H/V _{SET}
Unprotect BLOCK/Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	FIH	V _{SET}
Unprotect BLOCK/Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	DQH	H/V _{SET}
ERASE NV mode Register	LCR	30H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	COH	H
WRITE NV mode Register	LCR	40H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	X	H

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**UNITED STATES PATENT AND TRADEMARK OFFICE
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 22, Line 37, delete "After ERASE CONFIRM (DOH) is" and insert --After ERASE CONFIRM (DOH) is--

Column 24, Line 64, delete "A deep power-down mode is enable by" and insert --A deep power-down mode is enabled by--

Column 26, Line 15, delete "memory determines if nil blocks should" and insert --memory determines if all blocks should--

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